LISTING OF THE CLAIMS

The following is a complete listing of claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Previously Presented) A lateral bipolar CMOS integrated circuit comprising:

an inverter circuit comprising an n-channel MOS transistor and a p-channel MOS transistor, and having four terminals of:

a gate input terminal connected with the gates of the n-channel MOS transistor and the p-channel MOS transistor;

an output terminal connected with the drains of the n-channel MOS transistor and the p-channel MOS transistor;

a p-type base terminal connected with a p-type substrate of the n-channel MOS transistor; and

an n-type base terminal connected with an n-type substrate of the p-channel MOS transistor, wherein

the n-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an operation mode of an npn lateral bipolar transistor which is inherent in the n-channel MOS transistor, and

the p-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an operation mode of a pnp lateral bipolar transistor which is inherent in the p-channel MOS transistor;

a current source connected with the p-type base terminal of the n-channel MOS transistor; and

a current source connected with the n-type base terminal of the p-channel MOS transistor,

wherein currents from the current source connected with the p-type base terminal of the n-channel MOS transistor and the current source connected with the n-type base terminal of the p-channel MOS transistor are maintained at about 0 when the input voltage to the gate input terminal is approximately constant at a high level and constant at a low level; and

wherein a forward pulse current flows from the current source connected with the p-type base terminal of the n-channel MOS transistor to the p-type base terminal in synchronization to switching when the input voltage to the gate input terminal switches from the low level to the high level.

2. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 1, wherein the gate input terminal, the p-type base terminal and the n-type base terminal are input terminals of the inverter circuit, and the output terminal is an output terminal of the inverter circuit, and

the inverter circuit outputs, at the output terminal, a high-level or low-level voltage fed to the gate input terminal as an inverted level voltage.

3. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 2,

when the input voltage to the gate input terminal switches from the high level to the low level, a forward pulse current flows from the current source connected with the n-type base terminal of the p-channel MOS transistor to the n-type base terminal in synchronization to switching.

4. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 3, further comprising a voltage source and a ground source,

wherein the current source connected with the p-type base terminal of the n-channel MOS transistor is formed by a pull-up p-channel MOS transistor comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the p-type base terminal, and the source terminal and the substrate terminal are connected with the voltage source, and

the current source connected with the n-type base terminal of the p-channel MOS transistor is formed by a pull-down n-channel MOS transistor comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the n-type base terminal, and the source terminal and the substrate terminal are connected with the ground source.

5. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 1,

wherein the inverter circuit comprising the n-channel MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell.

6. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 2,

wherein the inverter circuit comprising the n-channel MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell.

7. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 3,

wherein the inverter circuit comprising the n-channel MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell.

8. (Previously Presented) The lateral bipolar CMOS integrated circuit according to claim 4,

wherein the inverter circuit comprising the n-channel MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell.

--END CLAIM RECITATION--

REMARKS

Favorable reconsideration of this application, in light of the following remarks, is respectfully requested.

Claims 1-8 are pending in this application, and claim 1 is independent.

Applicant notes with appreciation the Examiner's indication that the references cited in the Information Disclosure Statement (IDS) filed December 22, 2008 have been considered.

ENTRY OF AMENDMENT AFTER FINAL REJECTION

Entry of the Amendment is requested under 37 C.F.R. § 1.116 because the Amendment: a) places the application in condition for allowance for the reasons discussed herein; b) does not present any additional claims without canceling the corresponding number of final rejected claims; and/or c) places the application in better form for an appeal, if an appeal is necessary. Entry of the Amendment is thus respectfully requested.

SUMMARY OF EXAMINER INTERVIEW

Initially, Applicant wishes to thank Examiner O'Toole for her time during the telephone interview of July 23, 2009, the contents of which is summarized below.

During the course of the interview, proposed arguments with respect to the outstanding rejection of claim 1 were discussed. While no agreement was reached, the Examiner indicated that she will consider amendments/arguments that the Applicant submits in response to the outstanding Office Action.

Accordingly, the Examiner is respectfully requested to consider the argument presented below and kindly indicate her position with respect to them in the next Office communication.